SKYLINE ORBIT SEMICONDUCTOR

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GaN HEMT Technology: From Epitaxy to Power Device Integration

Speaker

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- ✓ Substrate Options
- ✓ Buffer Growth Techniques
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- ✓ Types of HEMT Architecture for Different Modes of Operation
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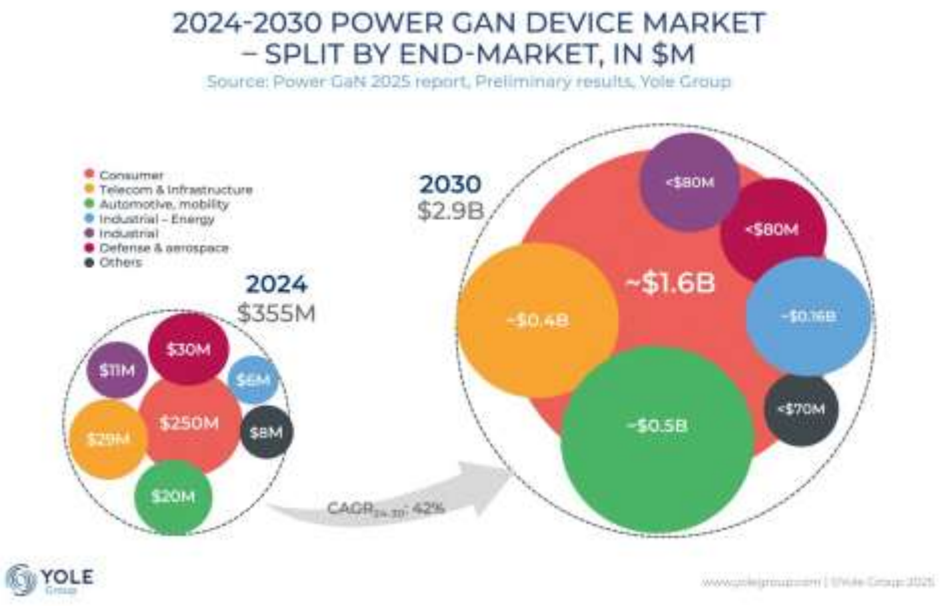
- ✓ F- ion doped Normally OFF GaN-MIS HEMT for High power applications

GaN Power Devices: Market Growth and Voltage-Domain Positioning



YOLE, 2025

- higher switching speed,
- higher efficiency
- higher power density

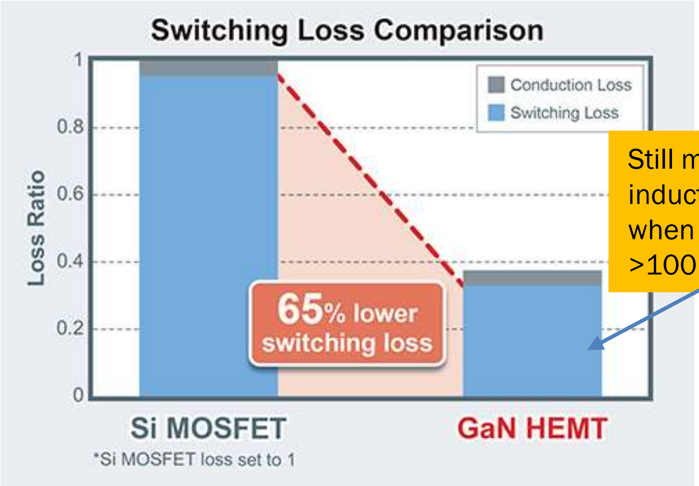
GaN owns low–mid voltage power; SiC rules high voltage.

GaN Power Device Positioning @650V:

Device Comparison (Comparison in the 650V band) Switching Efficiency

	Si SJ MOSFET	SiC MOSFET	GaN HEMT
Voltage range	500V to 1kV	600V to a few kV	**Less than 650V**
Large current	Better	Better	**Good**
High speed switching characteristic	Good	Better	**Excellent**
Ron·Qg *1	1 *2	0.63	**0.05**
Switching loss	1 *2	0.2	**0.1**

*1: index that represents switching performance. The lower the value, the better the switching performance. *2: Set Ron / Qg and switching loss of Si SJ MOSET to 1.



Still matters: Gate charge, parasitic inductances, operating voltage/current when it operates at high frequency >100kHz

- Low Conduction loss in HEMT (especially in D-mode) as Ron is less
- Current conduction is only via electrons → no minority carrier/inversion/**recovery phenomena** like in Si or SiC MOSFETs → switching loss is significantly reduced, though total switching loss also depends on device capacitances and circuit parasitic

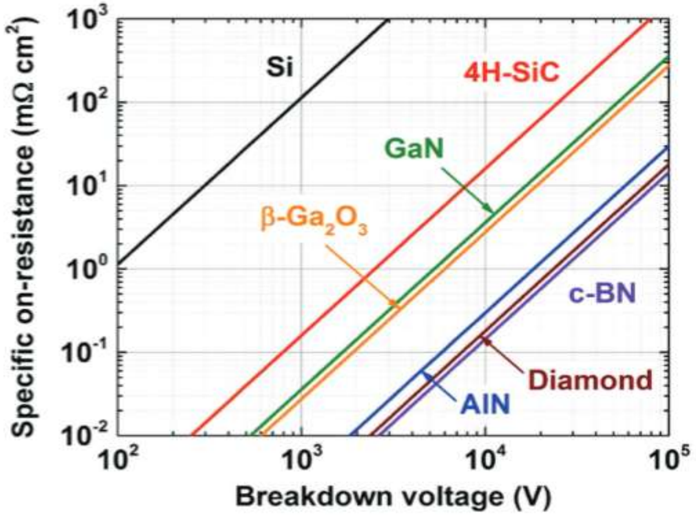
GaN Epitaxy

WBG Materials comparison

GaN (Gallium Nitride)

=A type of compound semiconductor material

	Si	4H-SiC	GaN
Bandgap (eV)	1.12	3.2	**3.4**
Dielectric constant	11.7	9.66	8.9
Breakdown field (MV/cm)	0.3	3	**3.3**
Electron saturation velocity (10^7 cm/s)	1	2	**2.5**
Electron mobility in the bulk (cm^2/Vs)	1350	720	900
Thermal conductivity (W/cm·K)	1.5	4.5	2 to 3

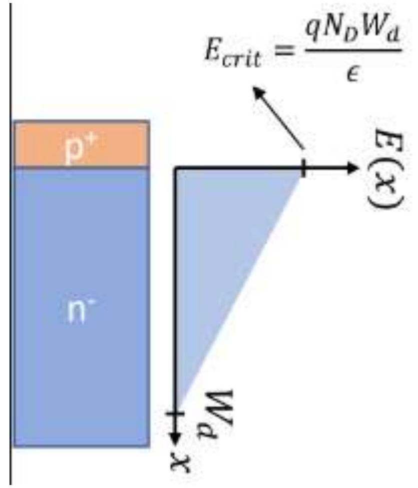


GaN is a great potential material that could contribute further energy saving compared to Si technology

*high breakdown field (3.3 MV/cm)
*high two-dimensional electron gas (2DEG) carrier mobility created in the HEMT (2,000 cm^2/V-s) enable low specific on-resistance ($R_{DS(on)}$).
Enables smaller devices with lower capacitances and reduced losses
*higher switching frequencies, which can lead to system cost, size and efficiency advantages.

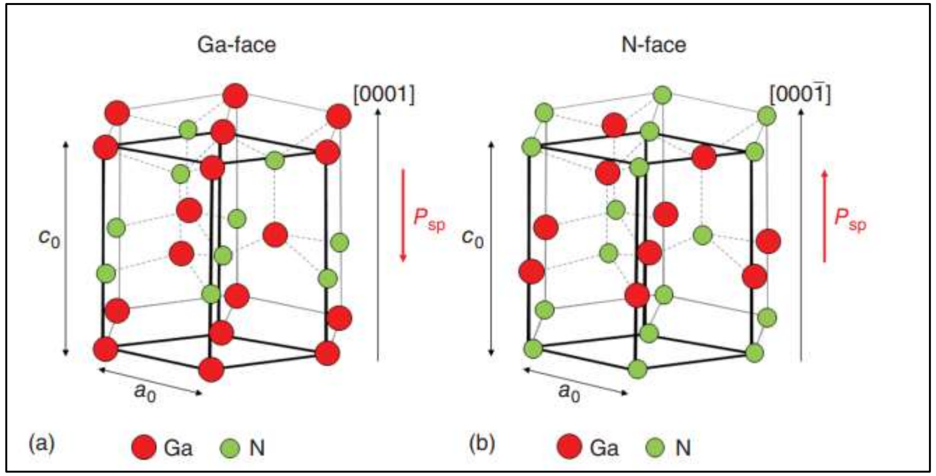
$$R_{ON} \propto 4V_{br}^2 / \mu \varepsilon E_{crit}^3$$

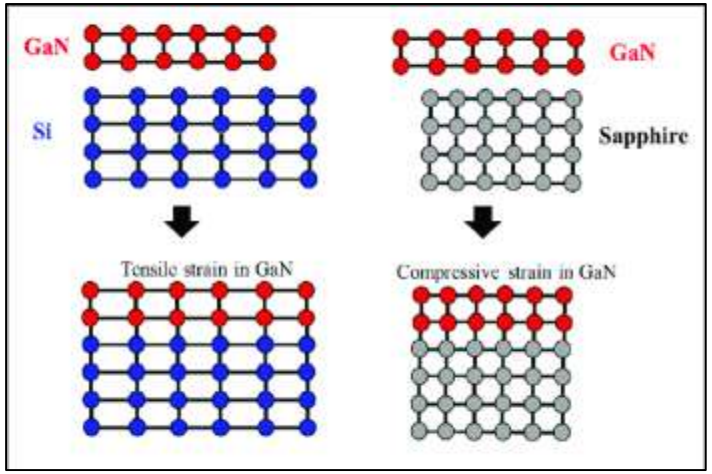
Material parameters that help minimizing the conduction losses in power transistors

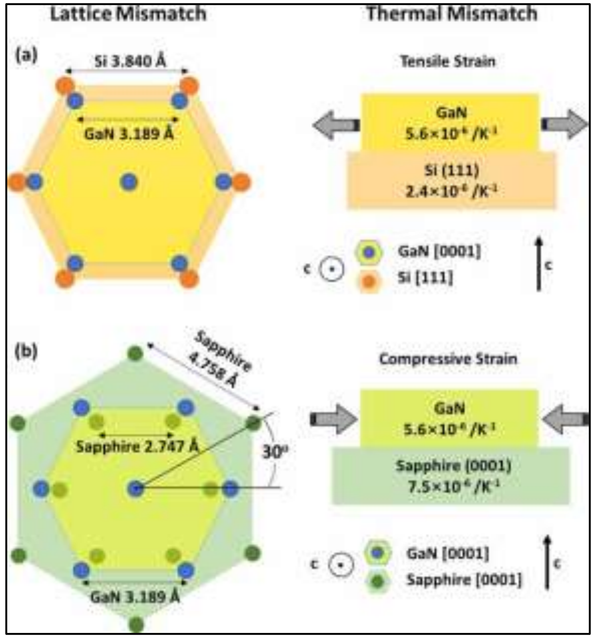


Crystal Structure and Epitaxy

- Crystal Structure







Parameters	AlN	GaN	InN
a_0 (Å)	3.1113	3.1878	3.537
c_0 (Å)	4.9814	5.1850	5.703

Wurtzite-> non-centrosymmetric along the c-axis – Lack of inversion symmetric along c-axis

Ga-Face:
Higher surface stability
Lower impurity incorporation
Preferred for HEMTs and LEDs

N-Face:
Good gate control,
Better RF performance
Difficult grow

Polarity affects surface chemistry, defect formation, and ultimately device performance—most power and RF devices use Ga-face GaN.

Substrate options

Properties and applications of GaN layers on different substrate	GaN-on-Al_2O_3	GaN-on-SiC	GaN-on-Si	GaN-on-GaN
Lattice mismatch (%)	16	3.5	−17	0
Thermal expansion coefficient mismatch, a_0 (%)	−34	21.4	53.5	0
Dislocation density (cm^{-2})	10^7–10^8	10^7–10^8	10^8–10^9	10^3–10^6
Device layout	Lateral	Lateral	Lateral	Lateral and vertical
Main application areas	Optoelectronics	HF electronics, optoelectronics	HF and power electronics	HF and power electronics, optoelectronics

Lattice and thermal mismatch set the defect density, which decides whether GaN is used for light, RF, or power

Lattice mismatch:

Formula: $\frac{\Delta a}{a} = \frac{a_{\text{film}} - a_{\text{substrate}}}{a_{\text{substrate}}} \times 100\%$

Thermal mismatch:

$$\Delta\alpha(\%) = \frac{\alpha_{\text{sub}} - \alpha_{\text{GaN}}}{\alpha_{\text{GaN}}} \times 100$$

GaN on sapphire

((7.5−5.6)/5.6)×100=− 34%

Tensile cracking during cool-down

Sapphire has poor heat dissipation compared to Si

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Buffer growth Techniques

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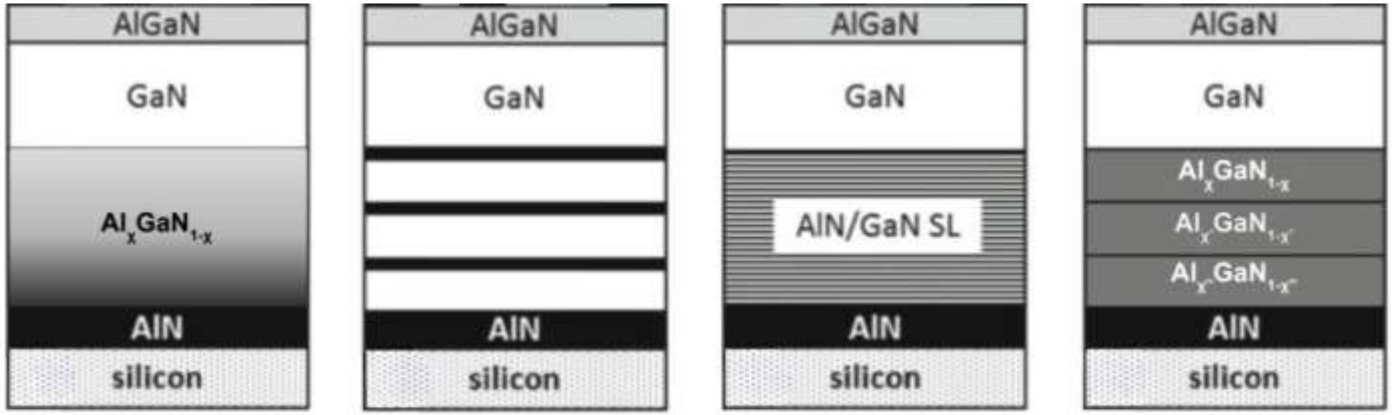
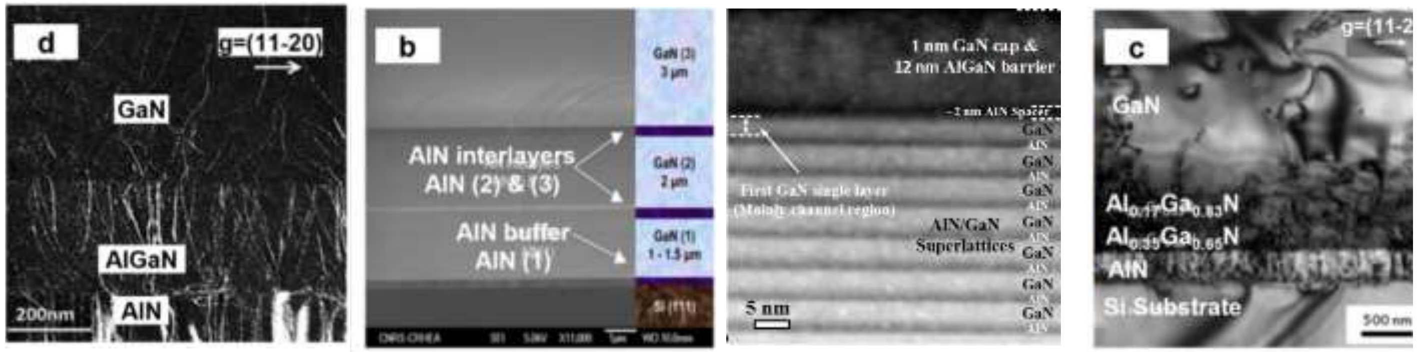
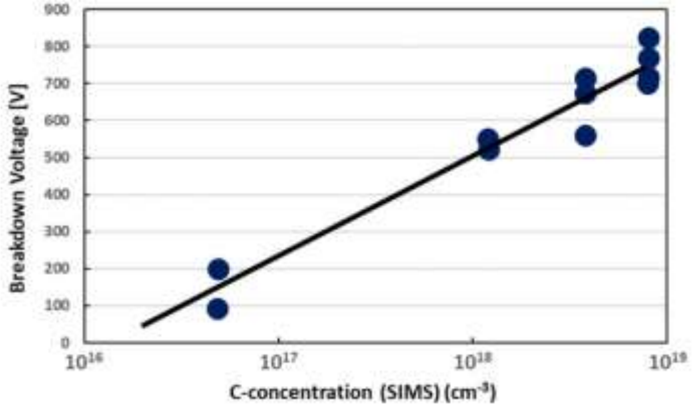
Thermal Mismatch ~54% and lattice mismatch ~17%



Graded Buffer | LT- AlN insertion | GaN/AlN SL | Step Graded Buffer



- Strain Accommodation: Reduces threading dislocation
- Diffusion Barrier: Prevents Ga–Si intermixing.
- Thermal Stress Mitigation: High thermal conductivity reduces wafer bowing and cracking.
- Surface Morphology Improvement: Promotes smooth 2D GaN growth for uniform device layers.
- Electrical Isolation: Wide bandgap (~6.2 eV) layer suppresses vertical leakage and improves buffer insulation.



Breakdown Voltage vs C doping

Enhance Breakdown Voltage by epitaxy

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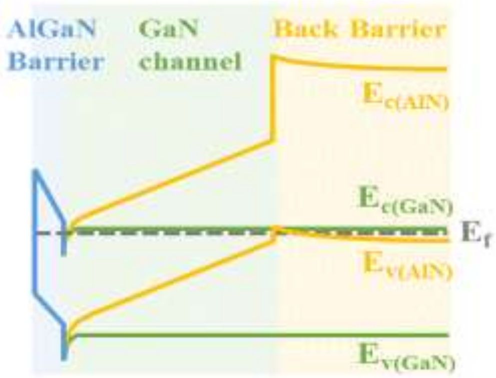
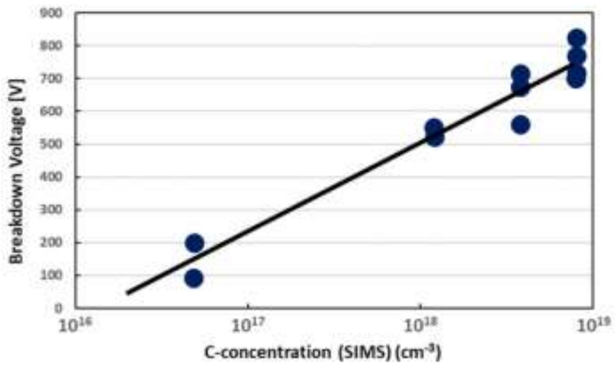
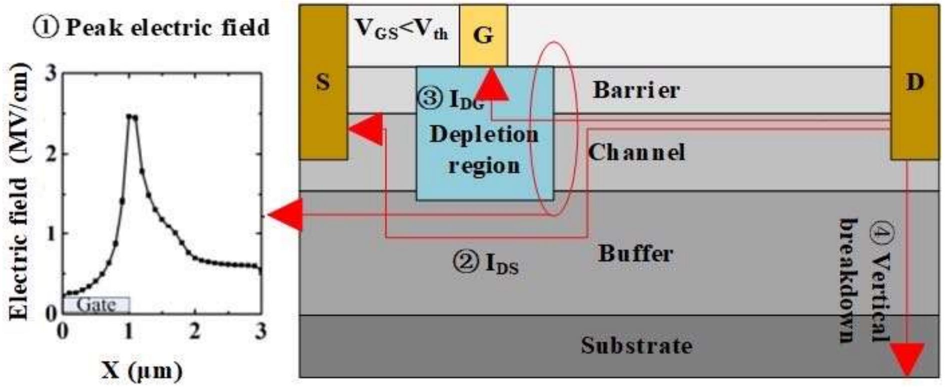


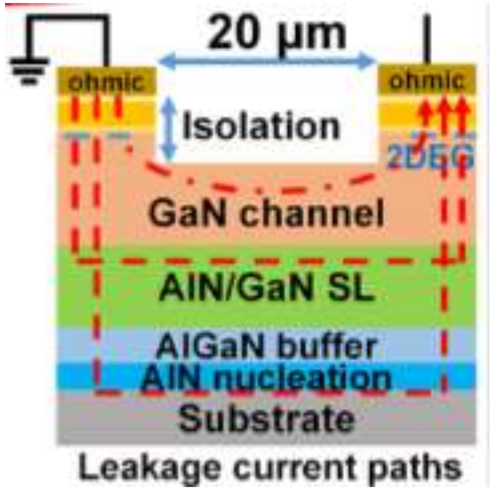


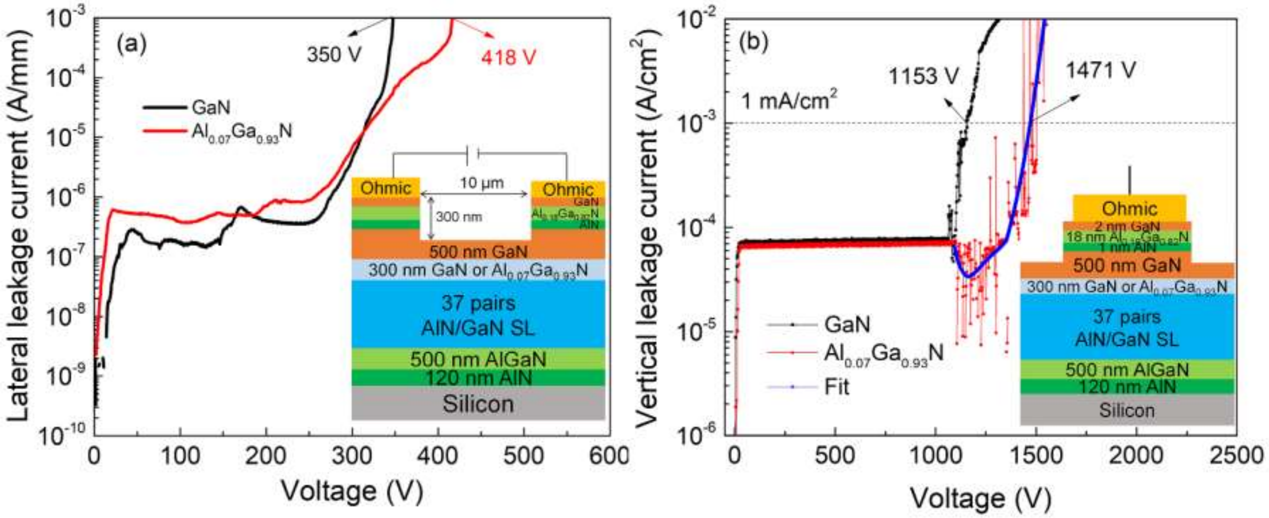


By introducing back Barrier

Breakdown Voltage vs C doping

Growing thick buffer layer

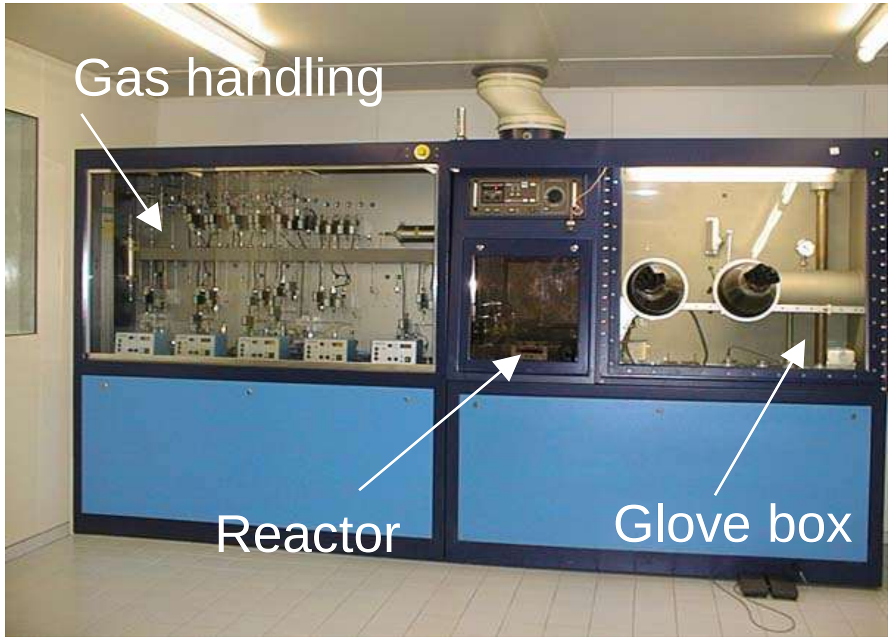




- SL reduces dislocations & smooths the surface → higher mobility.
- BB blocks electron leakage → higher breakdown voltage & lower contact resistance.
- Together, they create a high-quality, high-performance GaN HEMT on Si.

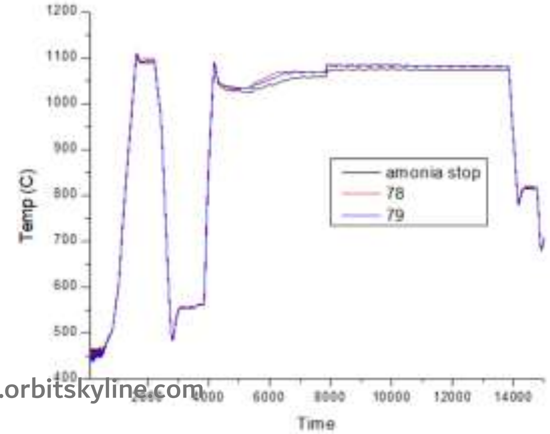
L T Hieu et al, Semicond. Sci. Technol. 39 (2024) 085006

MOCVD Overview



- Showerhead, planetary, vertical chamber
- T ~1300C
- In-situ tool1: Argus - Temp
- In-situ tools: EpiTT Reflectance

ARGUS = Advanced Real-time Growth Uniformity System



- Helps to monitor surface true temperature of wafer
- Control over temperature uniformity
- More useful for temperature sensitive materials integration such as AlGaN or InGaN

EpiTT: In-situ measurements system

Nucleation layer and its coalescence:

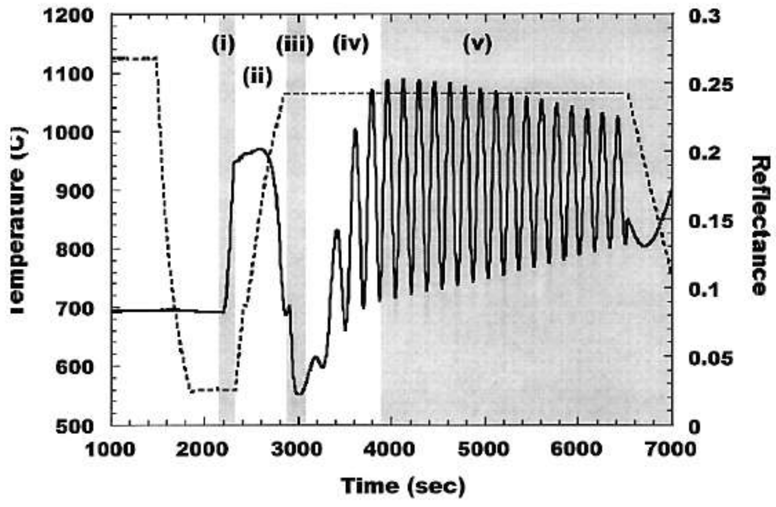


Fig. 1. Absolute reflectance (solid line) and temperature (dashed line) traces recorded during a typical growth of GaN on sapphire. Different stages of morphology evolution are shown in white and gray back-ground.

[Ng, J. Elec. Mat., 27 (1998)]

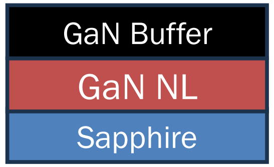
(i) LT GaN nucleation (surface n from 1.77 for sapphire to 2.5 for GaN) => increased reflectance (very thin layer so no time to see intensity decrease and further oscillations)

(ii) T° ramping until HT GaN growth => initial increase due to T° increase followed by decrease due to coarsening

(iii) HT nucleation

(iv) Recovery of reflectance due to coalescence

(v) (quasi) 2D growth mode



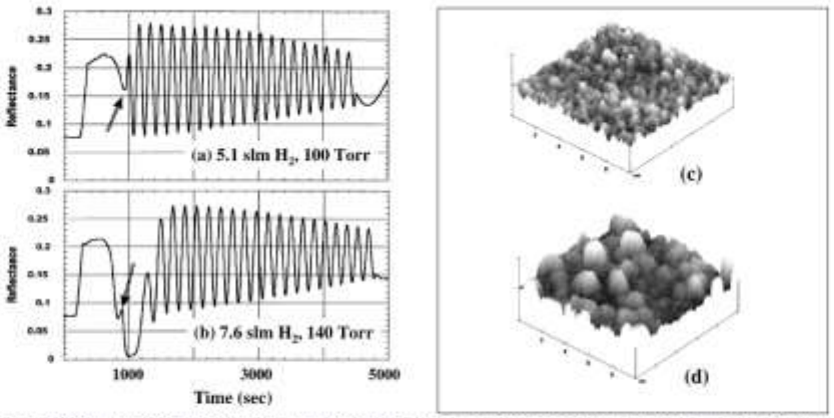


Fig. 3. (a) Reflectance trace of sample A, (b) reflectance trace of sample B. AFM images of the morphology of the nucleation layer (pointed by arrows in (a) and (b)) of Samples A and B are shown in (c) and (d), respectively.

Table I. Growth Parameters and Characterization Results of Samples A and B

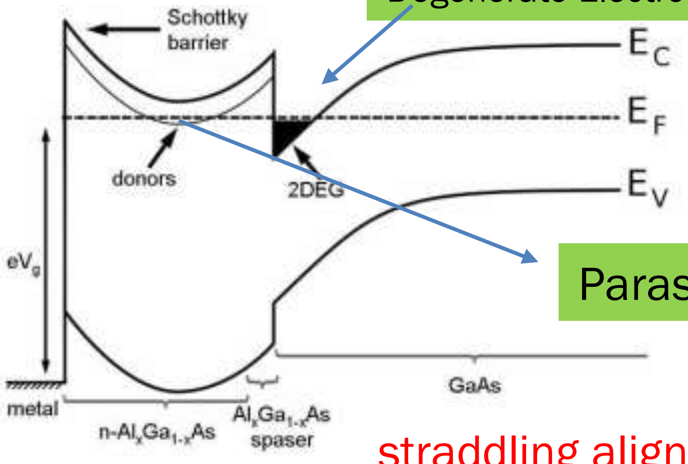
Sample	H_2 Flow Rate	Pressure (H_2)	Pressure (Total)	μ (cm^2/V-s)	n (cm^{-3})	X-Ray FWHM
A	5.1 slm	38 Torr	100 Torr	227	1.34×10^{17}	350"
B	7.6 slm	78 Torr	140 Torr	512	1.42×10^{17}	300"

Higher P (and higher H2 partial P) leads to rougher NL with bigger crystallites size => The further GaN layer on top has a better quality with the rougher NL (lower FWHM in XRD and much higher e- mobility)

GaN/AlGaN HEMT Device

HEMT GaAs/AlGaAs

Degenerate Electron Gas

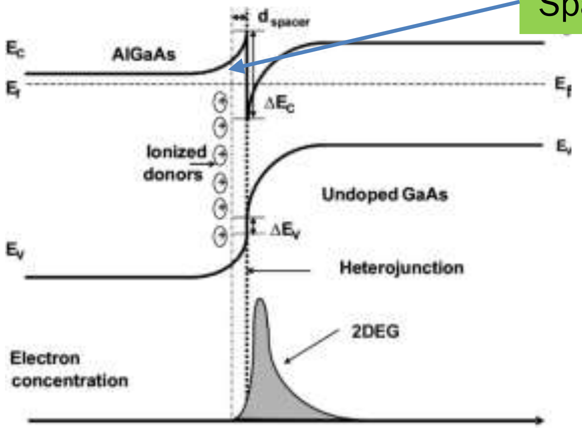


Parasitic channel

straddling alignment

Modulation doping is required: Dopants are placed in a barrier layer (AlGaAs), while carriers move into an adjacent undoped channel (GaAs).

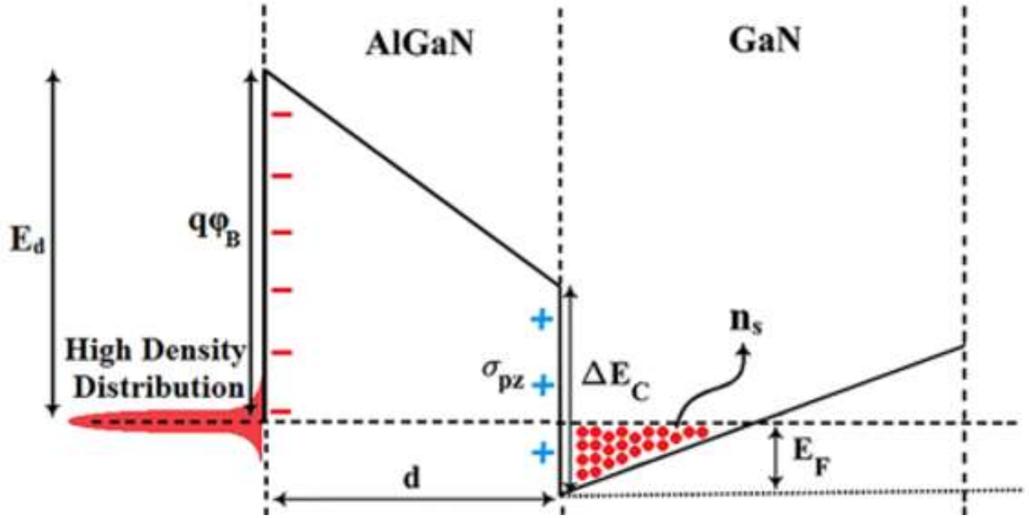
Spacer to avoid scattering



Spacer- helps to reduce the coulomb scattering

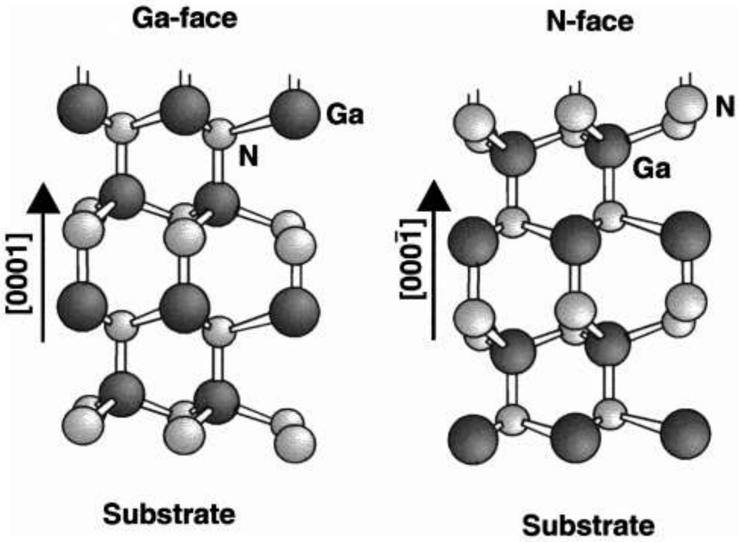
GaN/AlGaN

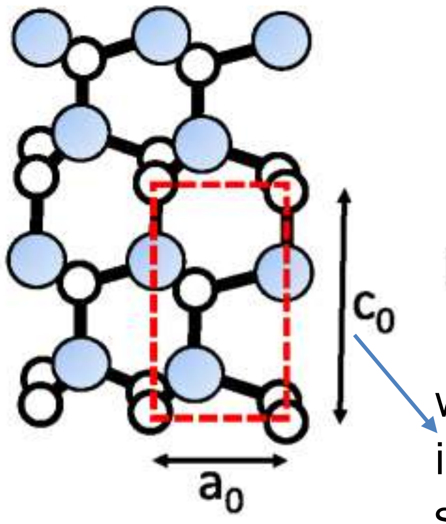
staggered alignment



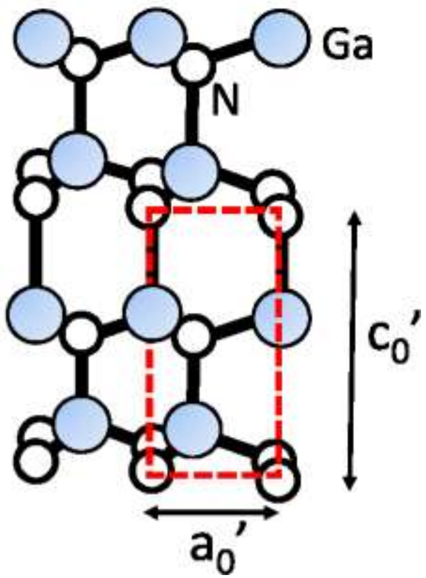
- No doping is required to create 2DEG
- No Dx centres present in GaN/AlGaN layers
- 2DEG created with the help of two different polarization in the material growth
- Barrier choices: AlGaN, AlN, InAlN and AlScN for better polarization

Spontaneous Polarization (Psp): Factor 1





wurtzite/
inversion
symmetry

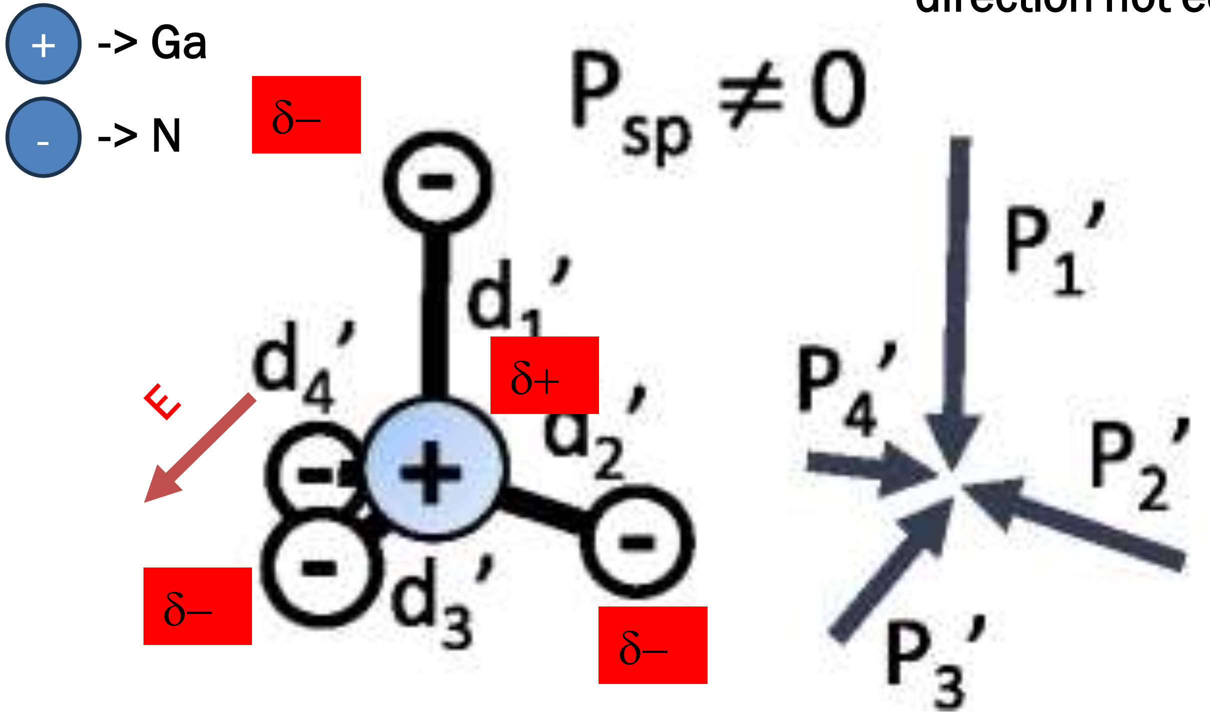


Distorted wurtzite/lack of inversion symmetry

Fujitsu Laboratories Ltd, Kobe, Japan

Spontaneous Polarization (Psp): Factor 2

Net polarization across Z direction not equals zero



N has high electronegativity than Ga
e- accumulation is high near the N, which creates Polarization (electric field)-> total polarization is not zero in C direction

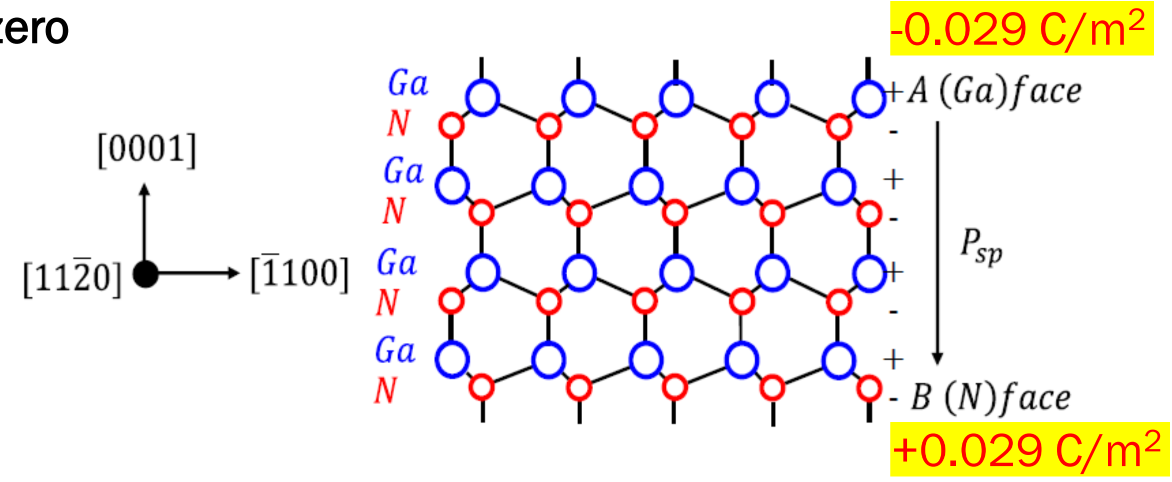


Figure: crystal structure of GaN, showing the sign and direction of the spontaneous polarization (adapted from https://doi.org/10.1116/1.590818)

Material	GaN (C m^{-2})	InN (C m^{-2})	AlN (C m^{-2})
P_{sp}	-0.029	-0.032	-0.081
P_{sp}	-0.034	-0.042	-0.090

Equivalent Electron density = Psp/q = 2E^{13}/cm^2

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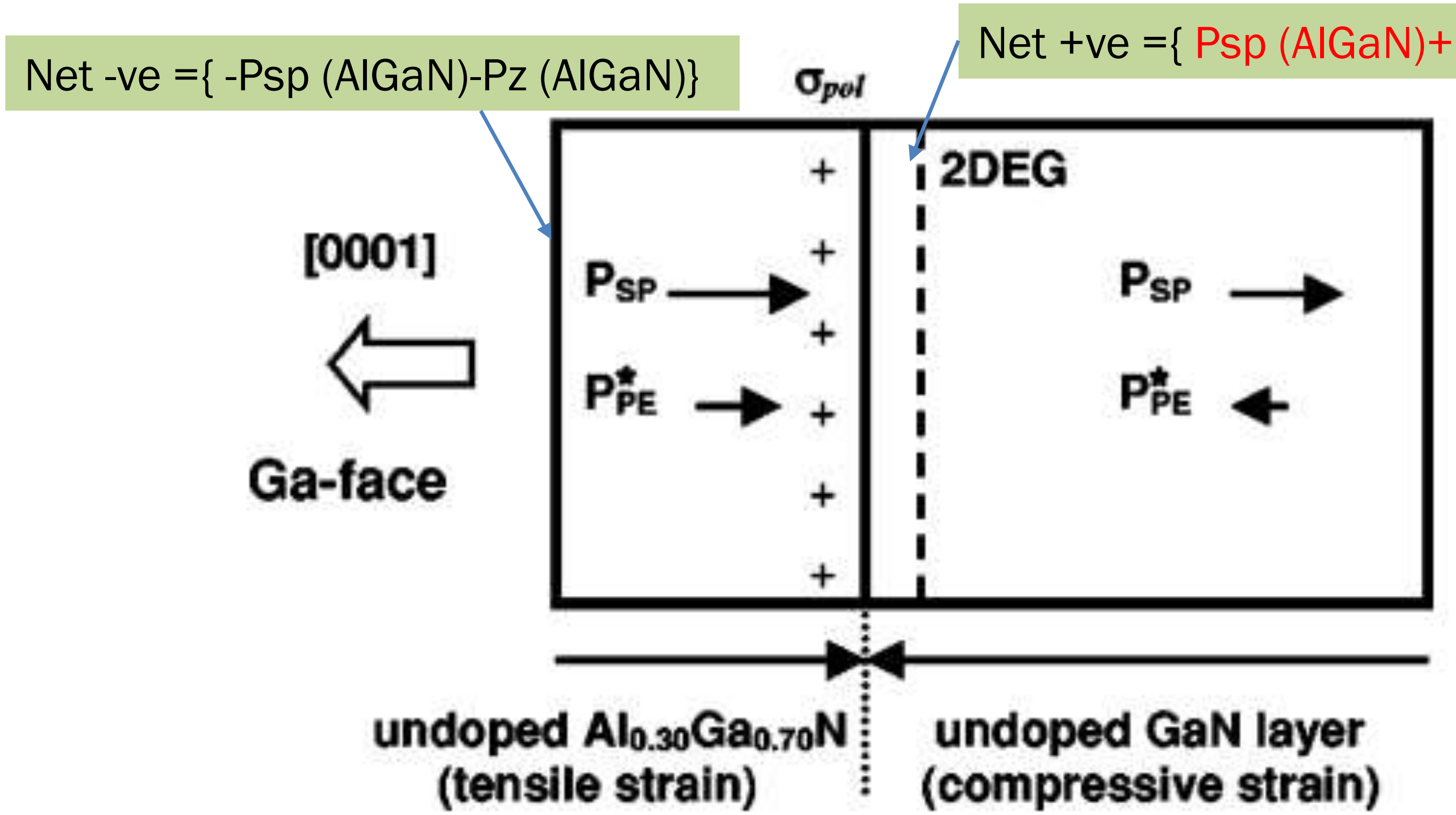
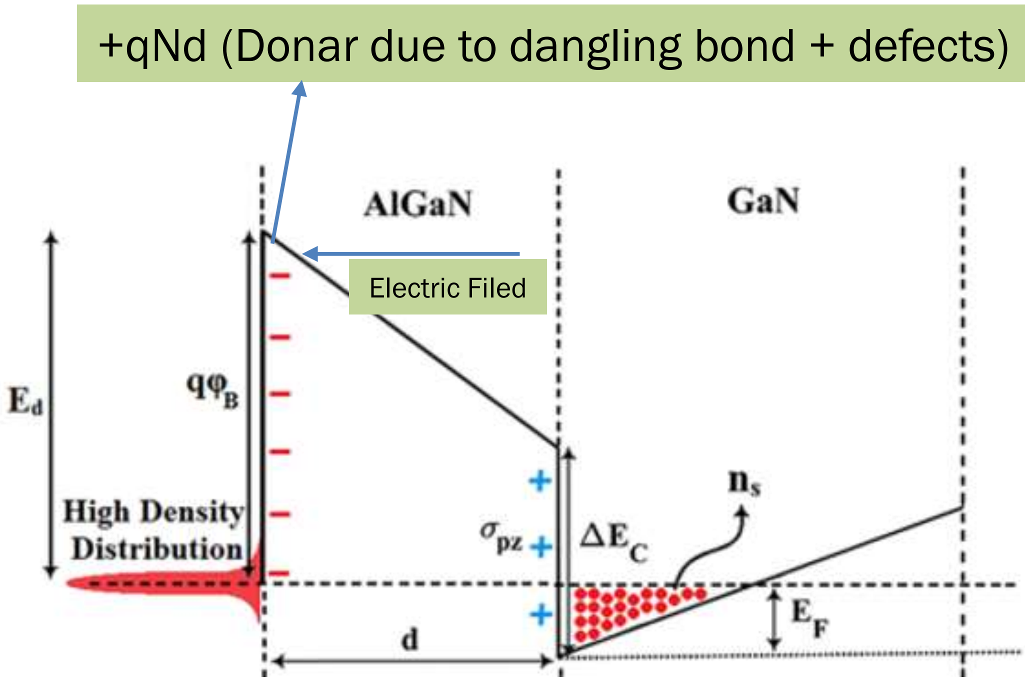
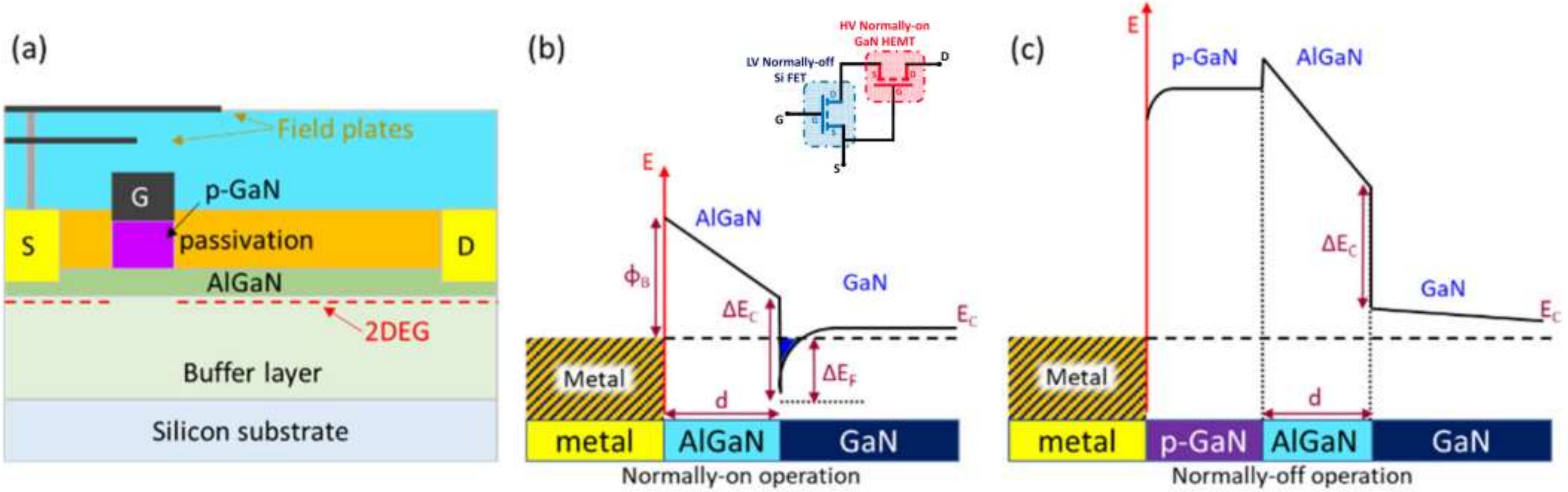
2DEG formation





Two-Dimensional Electron Gas (2DEG) comes from spontaneous and piezoelectric polarization, and confined by the quantum well.

Band alignement of E- and D-Mode devices



Sanna, “AlN/GaN MOS-HEMTs technology,”

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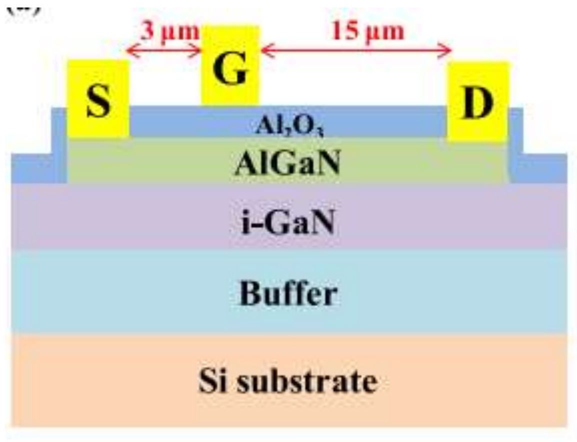
Types of HEMT Architecture for Different Modes of Operation

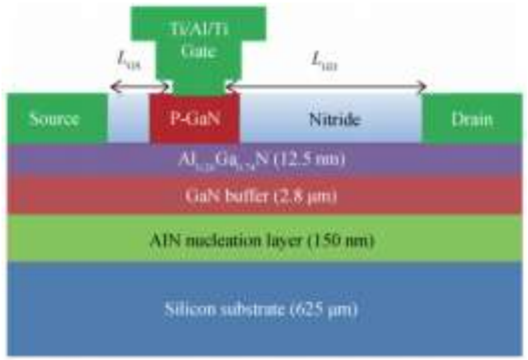
D-Mode (Depletion Mode)



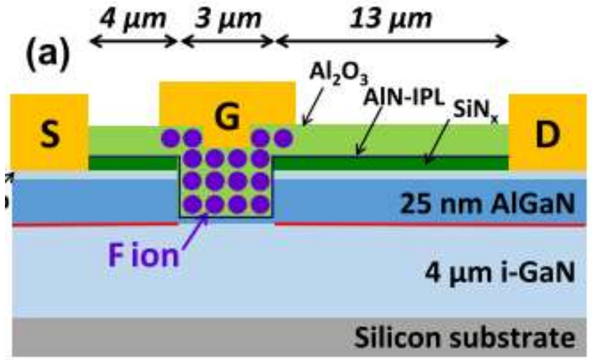
Normally ON MIS-HEMT

E-Mode (Enhancement mode)

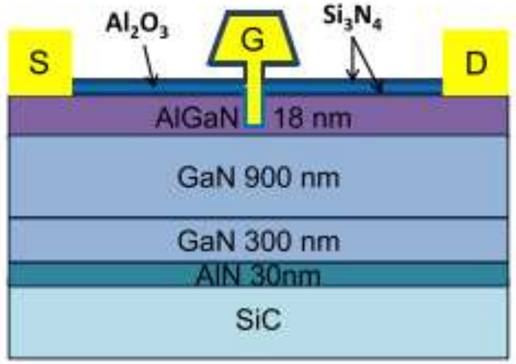
The F^-negative charge incorporation into the gate oxide stack



P-GaN



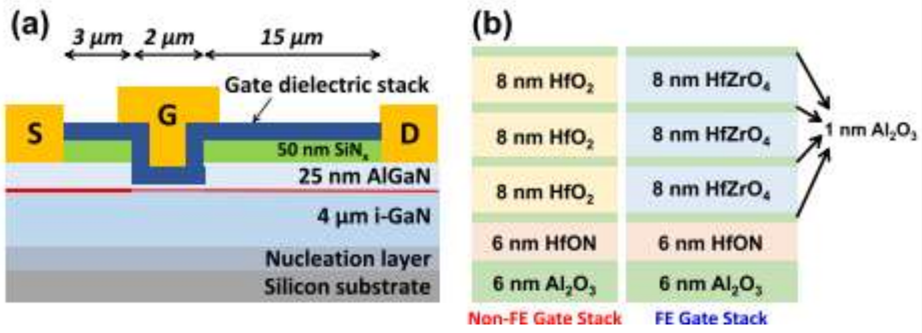
F^- Doped



Partially-Gate Recess MIS-HEMT

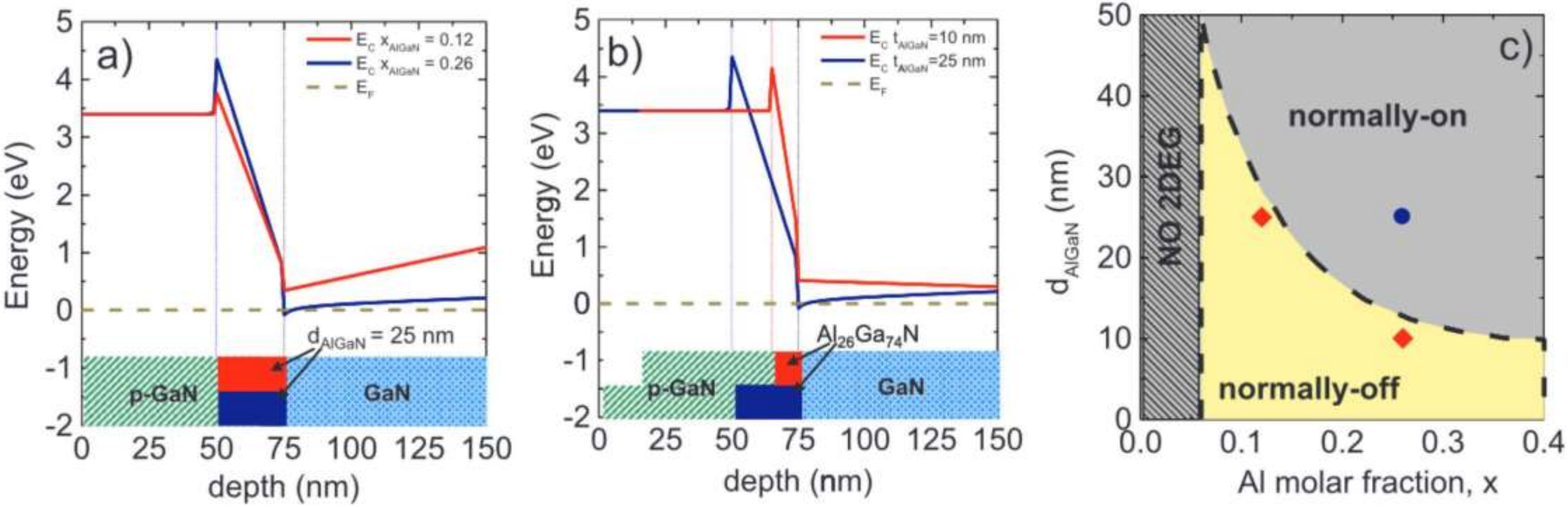
Normally OFF

- Higher **gate breakdown voltage**
- Better **Vth control**
- Improved **device reliability**



Ferroelectric Gate stack

Band alignement of E- and D-Mode devices



P-GaN raises the conduction band above the Fermi level and makes the device e-mode, with threshold voltages (Vt) typically in the 1.4- to 1.7-V range.

Sanna, “AlN/GaN MOS-HEMTs technology,”

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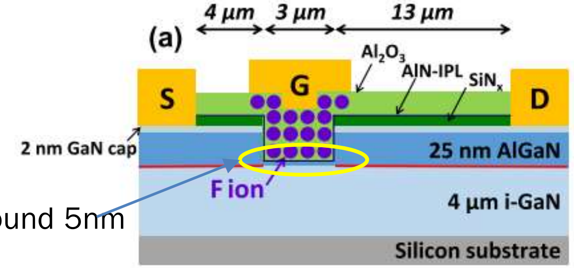
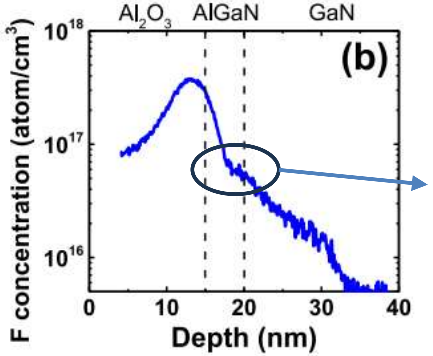
F- ion doped Normally OFF GaN-MIS HEMT for High power applications



AlN-interfacial passivation layer

Remaining barrier thickness around 5nm

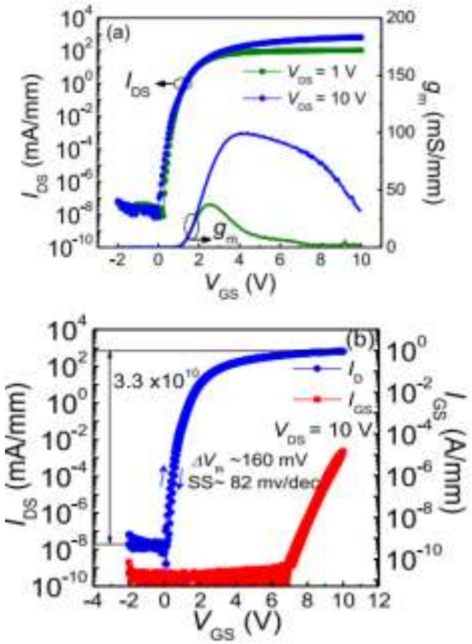


The implantation energy and ion dose were 10 keV and 1 × 10^{12} cm−2, respectively

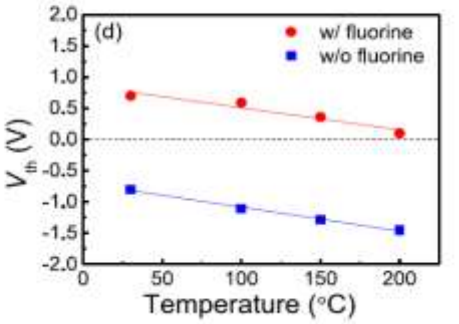
Trace of F- ions at the channel
Mobility reduces

(a) The schematic cross section of the F− doped GaN MIS-HEMTs. (b)Fluorine profiles measured by Secondary-Ion-Mass Spectrometry (SIMS) in F^- doped-Al_2O_3/AlGaN/GaN structure.

This approaches still lacks enough thermal stability evidence and also need Positive bias temperature instability (PBTI) results to verify the Vth stability.

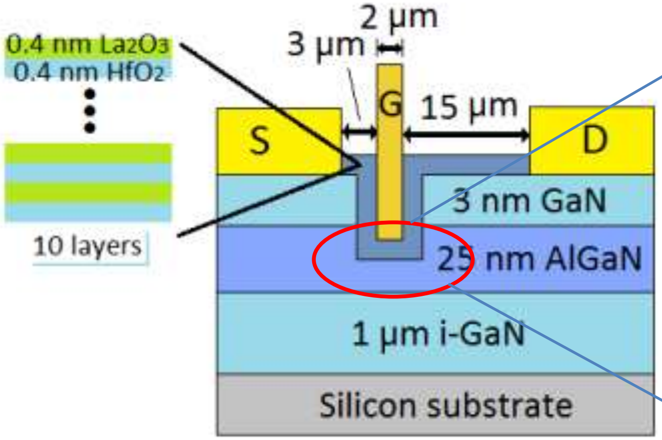


Transfer characteristics of the F− doped devices with various V_{DS} (a) and with constant V_{DS} = 10 V (b)

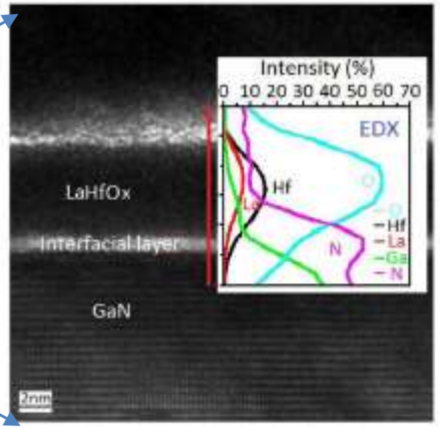


Temperature Instability

Enhancement Mode GaN-MIS HEMT for High power applications

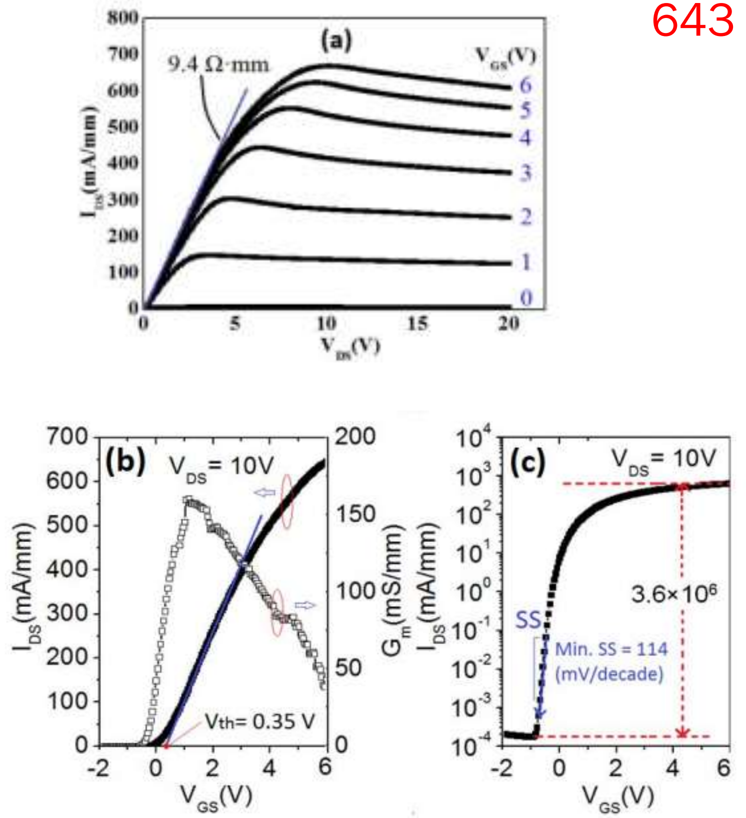


E-mode GaN MIS-HEMT with 10 layers of La_2O_3 (0.4-nm)/HfO2 (0.4-nm)



TEM image of the $LaHfO_x$/GaN layer

643 mA/mm



DC characteristics of the E-mode GaN MIS-HEMT with 8-nm LaHfOx gate insulator, (a) I_{DS}-V_{DS} curves, (b) I_{DS} & G_m vs. V_{GS} curves, and (c) transfer curve.

The current density and the ON-resistance are still poorer than the state-of-art normally-ON device

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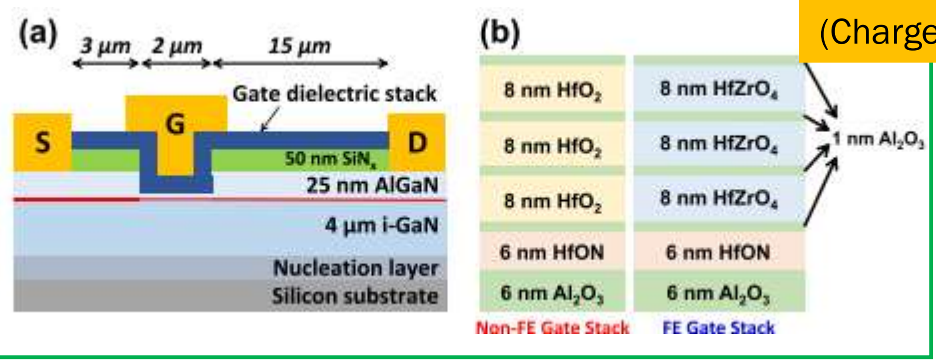
Enhancement Mode GaN-MIS HEMT for High power applications

Normally OFF

Ferroelectric Gate stack (Charge storage structure)



Combination of Gate-recess + Ferroelectric stack

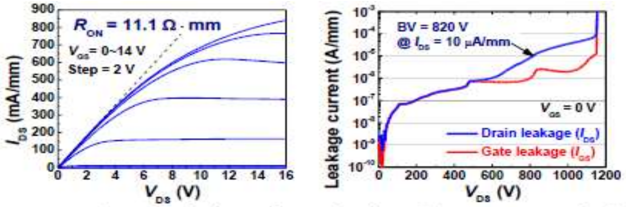


Fig. 5. (a) I_{DS}–V_{DS} characteristics of FE device. (b) OFF-state leakage current characteristics of FE device

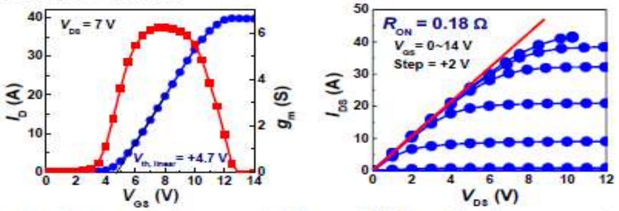
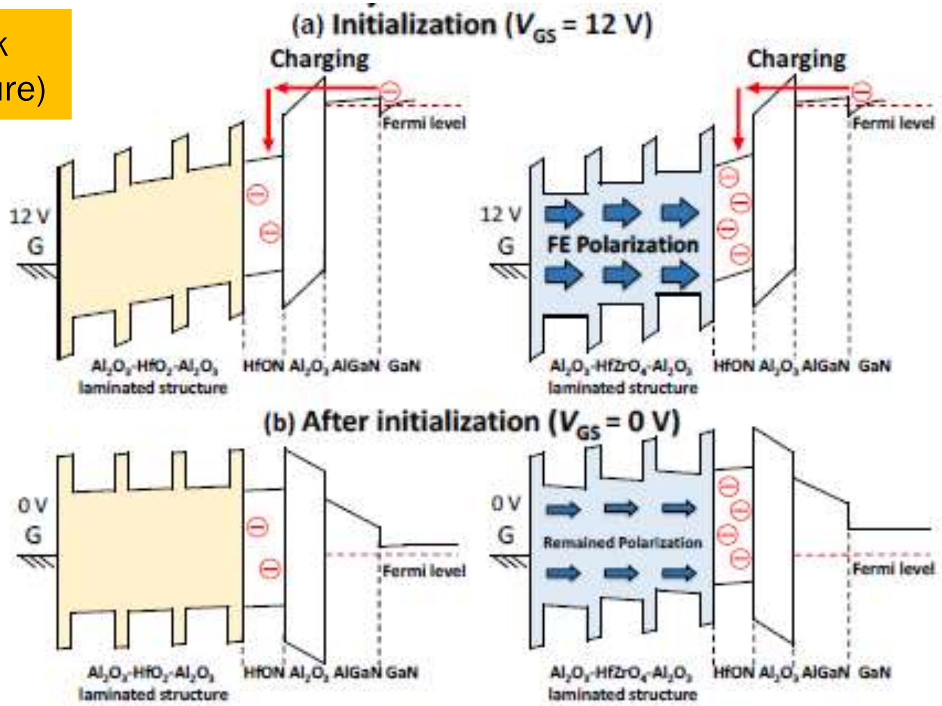


Fig. 6. (a) Pulsed I_{DS}-V_{GS} characteristics and (b) pulsed I_{DS}-V_{DS} characteristics of the fabricated 120-mm-gate-width FE devices. The pulse width and period were 100 μs and 10 ms, respectively.



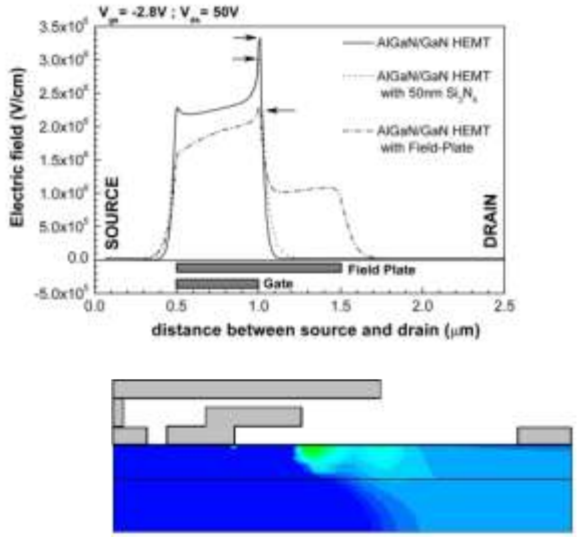
polarization hysteresis

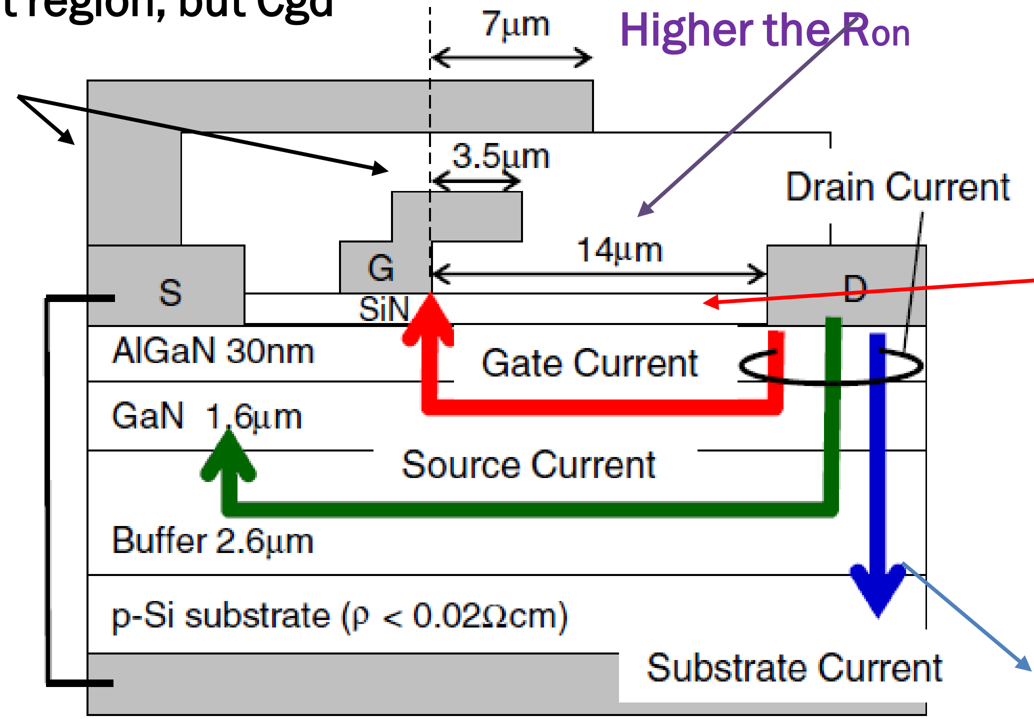
- FE layers can degrade with repeated switching.
- Polarization fatigue can shift V_{th} over time, causing device drift.
- Fabrication Complexity

Ways to Enhance V_{BR}

SCFP/GCFP : Alleviate peak E-field at gate edge, Shifts the electric filed deep into the drift region, but Cgd increases

Increasing L_{GD}: act as a drift region: which is directly propositional to the breakdown voltage of the device: Higher the distance, Higher the R_{on}





SiN ~20nm: In-situ or PECVD deposited Gate dielectric helps to reduce the gate leakage current: V_{BR} increases , surface trap reduces, improper optimization leads to current collapse

Buffer Leakage (Vertical or Lateral)
Critical in GaN-on-Si as Electrons leak through GaN buffer, Nucleation layers, Substrate interface Reach source via lateral conduction paths due to Insufficient Fe/C compensation

Vertical Breakdown: Highly resistive buffer/substrate helps to increase the vertical breakdown at high drain bias ~650V

Q/A

Thank You

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